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10/612,831	07/01/2003	Antonio Maria Borneo	851763.435	3911

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EXAMINER	
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ART UNIT	PAPER NUMBER
2192	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/612,831	BORNEO ET AL.	
	Examiner	Art Unit	
	Isaac T. Tecklu	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05/21/2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22 and 26-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22 and 26-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/21/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the amendment filed on 05/21/2007.
2. Claims 1-4, 7, 15 and 19 have been amended.
3. Claims 23-25 have been cancelled.
4. New claims 28-33 have been added.
5. Claims 1-22 and 26-33 have been examined.

Drawings

6. Figures 1-5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-11 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tang et al. (US 6,298,370 B1) in view of Stotzer (US 6,799,266 B1).

As per claim 1 (Currently Amended), Tang discloses process for executing programs on a multiprocessor system having a plurality of processors (e.g. FIG. 7 and related text), having an ~~given~~ instruction set architecture, each of ~~said~~ the processors being able to execute, at each processing cycle, a respective maximum number of instructions, characterized in that it comprises the operations of (col. 15: "... different instruction sets ..." and e.g. FIG. 7, CPU 106, DSP 1394 and FIG. 17, 1730 and related text):

~~compiling, at least in part,~~ retrieving a first set of ~~the~~ instructions ~~of said the programs~~ as compiled instruction words ~~of given~~ having a first length and executable on a first processor of said plurality (col. 3: 35-50"... first processor having an instruction set and a second processor having different instruction set ...processes the data according to the second processor ..." and (e.g. FIG. 21, VLIWDSP 2110 and related text); and

modifying, during runtime of one of said programs, at least some of said instruction words of ~~given length of the one of said programs~~ the first set of instructions converting them into modified-instruction words executable on a second processor of said plurality (col. 3:25-55 "... first processor sets up for at least part of the application program at run time ..." and col. 20:20-30 "... modified and compiled ..."), said modification operation in turn having at least one operation selected from the group of:

splitting said instruction words into modified-instruction words and managing a context of execution of the modified-instruction words by the second processor (col. 20:20-30 "... largely broken into fine granules ..." and col. 136: 15-25 "... dividing an application program into a plurality of granules..."); and

Tang does not explicitly disclose entering in the modified-instruction words no-operation instructions. However Stotzer discloses a method for reducing the size of code with an exposed

pipeline by encoding NOP (no operation instructions) as instruction operands .Therefore it would have been obvious to one skilled in the art at the time of the invention was made to combine Tang and Stotzer to compensate for instruction latencies and for reducing code size as once suggested by Stotzer (col. 1:35-45).

As per claim 2 (Currently Amended), Tang discloses the process according to claim 1, ~~further comprising:~~

~~compiling the instructions of said programs in part as first instruction words having a first given length and executable on said first processor of said plurality and in part as second instruction words of given length executable on a second processor of said plurality (col. 5: 45-50 "... operation placed in a tree-instruction by a VLIW compiler ..." and FIG. 3 and related text); modifying at least some of said first instruction words into first modified instruction words executable on said second processor of said plurality (col. 9: 58-65 "... translated into VLIWs at I-cache reload time ..."); and~~ further comprising:

retrieving a second set of instructions as compiled instruction words having a second length and executable on the second processor (col. 3: 35-50"... first processor having an instruction set and a second processor having different instruction set ...processes the data according to the second processor ..."); and

modifying at least some of ~~said second~~ the instruction words of the second set of instructions into second modified-instruction words executable on said first processor of said plurality (col. 128:35-55 "... running the first processor ... establishing second processor object..." and e.g. FIG. 95 and related text).

As per claim 3 (Currently Amended), Tang discloses the process according to claim 2, wherein said first set of instructions ~~instructions words~~ and said second set of instructions ~~instruction words~~ have, respectively, a first and a second maximum length with said first maximum length greater than said second maximum length (col. 3: 35-50"... first processor having an instruction set and a second processor having different instruction set ...processes the data according to the second processor ..." and e.g. FIG. 21, VLIWDSP 2110 and related text), the quotient between said first maximum length and said second maximum length having a

given value with the possible presence of a remainder and in that the procedure comprises the operations of (col. 88:50-65 "... remainder of this division producing a polynomial ..."):

selectively modifying instructions in the first set of instructions ~~said first instruction words by having said first maximum length into first modified-instruction words having said second maximum length~~ by (col. 128:35-55 "... running the first processor ... establishing second processor object..." and e.g. FIG. 95 and related text):

splitting said first instruction words into a number of said first modified-instruction words equal to the value of said quotient (col. 20:20-30 "... largely broken into fine granules ..." and col. 136: 15-25 "... dividing an application program into a plurality of granules..."); and

in the presence of said remainder, adding to said first modified-instruction words a further modified-instruction word of length equal to said second maximum length, said second maximum length being obtained by entering into said further first modified-instruction word a set of no-operation instructions (e.g. FIG. 24B and related text); and

selectively modifying ~~said~~ instructions in the first set of instructions ~~second instruction words by having said second maximum length into second modified-instruction words having said first maximum length~~ by (col. 128:35-55 "... running the first processor ... establishing second processor object..." and e.g. FIG. 95 and related text):

adding to said second instruction words of said second maximum length a number of no-operation instructions equal to the difference between said first maximum length and said second maximum length (e.g. FIG. 26 and related text).

As per claim 4 (Currently Amended), Tang discloses the process according to claim 1 ~~characterized in that it comprises the operations of~~ further comprising:

encoding said instructions on a given number of bits, said number of bits having a first bit identifying a length of instruction word executable on a processor of said plurality (e.g. FIG. 49 and related text);

associating to said given number of bits a respective appendix having a set of further bits identifying lengths of instruction words executable on different processors of said plurality (e.g. FIG. 49 and related text);

identifying for each of said instructions a processor of said plurality designed to execute said instruction, said identified processor being able to process for each processing cycle a given length of instruction word (col. 3: 35-50"... first processor having an instruction set and a second processor having different instruction set ...processes the data according to the second processor ..."); and

entering in the position of said first identifier bit a chosen bit between said further bits of said appendix, said chosen bit identifying the length of instruction word that can be executed by said identified processor (e.g. FIG. 52 and related text).

As per claim 5, Tang discloses the process according to claim 4, ~~characterized in that it comprises the operations of~~ further comprising the operation of erasing said respective appendix before execution of the instruction (e.g. FIG. 50 and related text).

As per claim 6, Tang discloses the process according to claim 4, ~~characterized in that~~ wherein said chosen bit is entered in the position of said first identifier bit in a step chosen from among: decoding of the instruction in view of the execution; re-filling of the cache associated to said identified processor; and decompression of the instruction in view of the execution (e.g. FIG. 122 and related text ").

As per claim 7 (Currently Amended), Tang discloses the process according to claim 1, further comprising:

alternatively distributing the execution of ~~the~~ instructions for programs ~~of said sequence~~ between the processors of said plurality, said instructions being directly executable by the processors of said plurality in conditions of binary compatibility (e.g. FIG. 124 and related text).

As per claim 8 (Currently Amended), Tang discloses the process according to claim 1, ~~characterized in that it comprises the operations of~~ further comprising the operation of selectively distributing the execution of said instructions among the processors of said plurality,

distributing dynamically the computational load of said processors (e.g. FIG. 125 and related text).

As per claim 9 (Currently Amended), Tang discloses the process according to claim 1, ~~characterized in that it comprises the operations of~~ further comprising the operation of selectively distributing the execution of said instructions between said processors of said plurality with the criterion of equalizing the operating frequency of the processors of said plurality (col. 30: 25-40 "... high frequency ...").

As per claim 10 (Currently Amended), Tang discloses the process according to claim 1, ~~characterized in that it comprises the operations of~~ further comprising the operation of performing a control process executed by at least one of the processors of said plurality so as to equalize its own workload with respect to the other processors of said multiprocessor system (col. 30: 25-40 "... high frequency ...").

As per claim 11 (Currently Amended), Tang discloses the process according to claim 1, ~~characterized in that it comprises the operations of~~ further comprising the operation of drawing up a table accessible by said control process, said table having items selected from the group of:

a list of processes being executed or suspended on any processor of said plurality of processors (col. 3: 35-50"... first processor having an instruction set and a second processor having different instruction set ...processes the data according to the second processor ...");

the progressive number thereof according to the order of activation; the percentage of maximum power of the processor that is used by said process (col. 17: 15-25 "... computing power ...");

the execution time, said time, if zero, indicating that the process is temporarily suspended from being executed (col. 20: 40-55 "... resource is suspended ...");

the amount of memory of the system used by the process to be able to execute the function for which it is responsible (col. 21: 55-65 "... system memory space ...");

the maximum length of the long instruction that the VLIW processor can execute and for which it had been generated during compiling (e.g. FIG. 21, VLIWDSP 2110 and related text);

maximum length of the long instruction of the VLIW processor on which it is executed (e.g. FIG. 21, VLIWDSP 2110 and related text); and

the address of the portion of memory in which the data and the instructions are stored (col. 24:20-35 "... current address of the allocated memory ...").

As per claim 26 (New), Tang discloses the process according to claim 1, further comprising:

executing, by the second processor, the modified instruction words (e.g. FIG. 39 and related text).

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

9. Claims 12-22 and 27-32 are rejected under 35 U.S.C. 102(a) as being anticipated by Tang (US 6,298,370 B1).

As per claim 12 (Currently Amended), Tang discloses a multiprocessor system (e.g. FIG. 6 and related text), configured for operating with the process according to Claim 1, comprising:

a first processor having a given instruction set architecture and configured to execute programs with instruction words of a first length (col. 3: 35-50"... first processor having an instruction set and a second processor having different instruction set ...processes the data according to the second processor ...");

a second processor having the given instruction set architecture and configured to execute programs with instruction words of a second length; (col. 3: 35-50"... first processor having an

instruction set and a second processor having different instruction set ...processes the data according to the second processor ...");

means for converting instruction words of the first length compiled for execution on the first processor into modified instruction words of the second length executable on the second processor (col. 31: 40-55).

As per claim 13 (Currently Amended), Tang discloses the multiprocessor system according to claim 12, ~~characterized in that~~ wherein said processors are all of the VLIW type (e.g. FIG. 21, VLIWDSP 2110 and related text).

As per claim 14 (Currently Amended), Tang discloses the multiprocessor system according to claim 12, ~~characterized in that~~ wherein said plurality of processors comprises at least one VLIW processor (e.g. FIG. 21, VLIWDSP 2110 and related text).

As per claim 15 (Currently Amended), Tang discloses a system comprising:

a plurality of processors coupled for receiving compiled instruction sets (e.g. FIG. 6, element 606, FIG. 16, element 706 and related text);

a first processor of the plurality coupled to each of the other processors within said plurality, said first processor receiving from the other processors data representative of the workload of each of said other processors (col. 3: 35-50"... first processor having an instruction set and a second processor having different instruction set ...processes the data according to the second processor ...");

an output signal from said first processor to said instruction set stream, said output signal controlling the instructions, which are sent to each of said processors based on the results of the workload measurement of said processors (e.g. FIG. 21, VLIWDSP 2110 and related text).

As per claim 16, Tang discloses the system according to claim 15, wherein said workload measurement comprises power consumption of each of said processors of said plurality (e.g. FIG. 6 and related text).

As per claim 17, Tang discloses the system according to claim 15, wherein said workload measurement comprises memory usage of each of said processors of said plurality (col. 21: 55-65 "... system memory space ...").

As per claim 18, Tang discloses the system according to claim 15, wherein said workload measurement comprises number of operations carried out by each of said processors of said plurality (col. 21: 55-65 "... system memory space ...").

As per claim 19 (Currently Amended), Tang discloses a process of directing instruction sets to be executed by a plurality of processors in a system comprising:

receiving a plurality of executable instruction sets on a bus line connected to said processors (e.g. Fig. 1 and related text);

receiving workload data at a first processor of said plurality of processors, said workload data being representative of workload of each of the processors of said plurality (col. 3: 35-50"... first processor having an instruction set and a second processor having different instruction set ...processes the data according to the second processor ...");

comparing the workload of each of the processors (e.g. Fig. 124 and related text); and

sending a signal from said first processor based on the data representative of the workload of each of the processors of said plurality to the bus line for modifying the number of executable instruction sets sent to each processor based on their respective workloads (e.g. FIG. 21, VLIWDSP 2110 and related text).

As per claim 20, Tang discloses the process according to claim 19, wherein said workload data includes data regarding power consumption of each of said processors of said plurality (e.g. FIG. 14 and related text).

As per claim 21, Tang discloses the system according to claim 19, wherein said workload data includes data regarding memory usage of each of said processors of said plurality (e.g. FIG. 14 and related text).

As per claim 22, Tang discloses the system according to claim 19, wherein said workload data includes data regarding the number of operations carried out by each of said processors of said plurality (e.g. FIG. 14 and related text).

As per claim 28 (New), Tang discloses the multiprocessor system of claim 12, further comprising:

means for selectively controlling execution of the modified instruction words by the second processor (e.g. FIG. 7 and related text).

As per claim 27 (New), Tang discloses the multiprocessor system according to claim 12 wherein said means for converting instruction words of the first length compiled for execution on the first processor into modified instruction words of the second length executable on the second processor comprises converting the instruction words during runtime (col. 3: "... first processor sets up for at least part of the application program at run time ...").

As per claim 29 (New), Tang discloses the system of claim 15 wherein the first processor is configured to manage a context of program execution for each of the processors in the plurality of processors (e.g. FIG. 7, 106 and related text)

As per claim 30 (New), Tang discloses the system of claim 29 wherein managing a context of program execution includes tracking addresses in a memory in which data and instructions are stored (e.g. FIG. 51B and related text)

Per claim 31 (New), Tang discloses the process of claim 19, further comprising: managing a context of program execution for each of the processors in the plurality of processors (col. 16: 60-67 "... from the address of the first byte ...").

Per claim 32 (New), Tang discloses the process of claim 19, further comprising:

modifying a set of compiled instructions sent to a processor in the plurality of processors by splitting instruction words in the set of compiled instructions into modified instruction words (col. 20:20-30 "... largely broken into fine granules ..." and col. 136: 15-25 "... dividing an application program into a plurality of granules...").

10. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tang et al. (US 6,298,370 B1) in view of Stotzer (US 6,799,266 B1).

Per claim 33 (New), Tang discloses the process of claim 19, further comprising:

Tang does not explicitly disclose adding no-operation instruction words to the instruction words in the set of compiled instructions. However Stotzer discloses a method for reducing the size of code with an exposed pipeline by encoding NOP (no operation instructions) as instruction operands .Therefore it would have been obvious to one skilled in the art at the time of the invention was made to combine Tang and Stotzer to compensate for instruction latencies and for reducing code size as once suggested by Stotzer (col. 1:35-45).

Response to Arguments

11. Applicant's arguments with respect to claims 1-22 and 26-33 have been considered but are moot in view of the new ground(s) of rejection. See art made of record Tang et al. (US 6,298,370 B1) and Stotzer (US 6,799,266 B1).

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Isaac T. Tecklu whose telephone number is (571) 272-7957. The examiner can normally be reached on M-TH 9:300A - 8:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TUAN DAM
SUPERVISORY PATENT EXAMINER

Isaac Tecklu
Art Unit 2192